Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended): A method for reading data from a synchronous memory of the type having data cells arranged in rows and columns and having a single row cache, comprising:

arranging said synchronous memory in a symmetrical layout to include a left plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block; a centrally located single row cache; and a right plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two;

receiving an initial command and row address data for reading contents of a row of said synchronous memory selected by said row address data, said reading being performed exclusive of column address data;

moving said contents of said row into said single row cache;

after said contents of said row have been moved into said single row cache, receiving a "read" command and column address data; and

in response to said "read" command, reading data from said single row cache at a column address specified by said column address data for output by said synchronous memory.

2. (Original): The method of claim 1 wherein said initial command is received substantially concurrently with said row address data.

3. (Original): The method of claim 1 wherein said "read" command and said column address data are received substantially concurrently.

4. (Previously presented): The method of claim 1 further comprising moving said data read from said single row cache to an output of said synchronous memory after a predetermined number of clock cycles after said "read" command.

5. (Previously presented): The method of claim 4 wherein moving said data read from said row cache to an output of said synchronous memory after a predetermined number of clock cycles comprises moving said data read from said single row cache to an output of said memory after two clock cycles.

6. (Original): The method of claim 4 wherein said predetermined number of clock cycles is two.

7. (Original): The method of claim 1 wherein said receiving an initial command comprises receiving a "bank activate" command.

8. (Original): The method of claim 1 further comprising performing a first precharging operation prior to receiving said initial command.

9. (Previously presented): The method of claim 4 further comprising initiating a memory operation after said contents of said row have been moved into said single row cache and before said data read from said single row cache has been moved to said output of said synchronous memory.

10. (Currently amended): The method of claim 9 wherein said memory operation ~~is~~ comprises a precharging operation.

11. (Currently amended): The method of claim 9 wherein said synchronous memory ~~is~~ comprises a SDRAM array.

12-27. (Canceled)

28. (New): A synchronous memory comprising:

a plurality of first memory blocks;

a first row decoder to access a row of data in the first memory blocks in response to a row address;

a row cache configured to receive and to store therein an entire row of data from the first memory blocks; and

a column decoder to access data stored in the row cache in response to a column address,

wherein the row cache is capable of receiving and storing the entire row of data from the first memory blocks absent the column address.

29. (New): The synchronous memory of claim 28 further comprising a plurality of second memory blocks and a second row decoder to access a row of data in the second memory blocks in response to a row address, the row cache and the column decoder being disposed between the first memory blocks and the second memory blocks.

30. (New): The synchronous memory of claim 28 wherein at least some of the first memory blocks are paired off to define pairs of memory blocks, the synchronous memory further comprising a plurality of first sense amplifier sets, each pair of memory blocks being associated with one the first sense amplifier sets.

31. (New): The synchronous memory of claim 30 wherein at least some of the second memory blocks are paired off to define pairs of memory blocks, the synchronous memory further comprising a plurality of second sense amplifier sets, each pair of memory blocks among the second memory blocks being associated with one the second sense amplifier sets.

32. (New): The synchronous memory of claim 28 further comprising means for performing a first precharging operation prior to receiving said "bank activate" command.

33. (New): The synchronous memory of claim 28 further comprising means for performing a second precharging operation after said "bank activate" command and prior to said "read" command.

34. (New): An SDRAM comprising the synchronous memory of claim 28.

35. (New): The SDRAM of claim 34 wherein the row decoder is capable of accessing a row among the first memory blocks in response to a "bank activate" command.

36. (New): The SDRAM of claim 34 wherein the column decoder is capable of accessing data in the row cache in response to a "read" command.

37. (New): The SDRAM of claim 34 further comprising an output to which data read from the row cache is moved, the data being moved to the output of the SDRAM a predetermined number of clock cycles after the "read" command.

38. (New): The SDRAM of claim 37 wherein the predetermined number of clock cycles comprises two clock cycles.

39. (New): A memory device comprising:

first memory blocks;

second memory blocks;

a cache disposed between the first memory blocks and the second memory blocks, the cache configured to latch a selected row of data read out from the first memory blocks and a selected row of data read out from the second memory blocks; and

data buses coupling the selected row of data read out from the first memory blocks and the selected row of data read out from the second memory blocks into the cache,

data latched in the cache being accessed from the first memory blocks and the second memory blocks absent a column address.

40. (New): The memory device of claim 39 further comprising a first row decoder to access a row of data from the first memory blocks and a second row decoder to access a row of data from the second memory blocks.

41. (New): The memory device of claim 40 further comprising a column decoder to access selected data stored in the cache in response to a column address.

42. (New): The memory device of claim 39 wherein the cache is capable of latching an entire selected row of data from the first memory blocks and latching an entire selected row of data from the second memory blocks.